–	86	capacitor.ti. and(second near polarity)) and(first near polarity	USPAT; US-PGPUB; JPO	2004/10/18 13:28
–	73	((capacitor.ti. and(second near polarity)) and(first near polarity)) and(terminal$1)	USPAT; US-PGPUB; JPO	2004/10/18 13:29
–	57	(((capacitor.ti. and(second near polarity)) and(first near polarity)) and(terminal$1)) and(electrode or plate)	USPAT; US-PGPUB; JPO	2004/10/18 13:29
–	1	((((capacitor.ti. and(second near polarity)) and(first near polarity)) and(terminal$1)) and(electrode or plate)) and(anode)	USPAT; US-PGPUB; JPO	2004/10/18 13:29
–	27	((((capacitor.ti. and(second near polarity)) and(first near polarity)) and(terminal$1)) and(electrode or plate)) and(anode or positive)	USPAT; US-PGPUB; JPO	2004/10/18 13:29
–	23	(((((capacitor.ti. and(second near polarity)) and(first near polarity)) and(terminal$1)) and(electrode or plate)) and(anode or positive)) and(cathode or negative)	USPAT; US-PGPUB; JPO	2004/10/18 14:47
–	9	capacitor near package.ti. and(terminal$1)	USPAT; US-PGPUB; JPO	2004/10/18 14:49
–	22	capacitor.ti. and(second near polarity near terminal$1)	USPAT; US-PGPUB; JPO	2004/10/19 08:57
–	415	storage with capacitor.ti.	USPAT; US-PGPUB; JPO	2004/10/19 08:57
–	29	361/$.ccls. and storage with capacitor.ti.	USPAT; US-PGPUB; JPO	2004/10/19 09:25
–	0	MLc with capacitor.ti. and(anode)	USPAT; US-PGPUB; JPO	2004/10/19 09:25
–	15	multilayer with capacitor.ti. and(anode)	USPAT; US-PGPUB; JPO	2004/10/19 09:26
–	13	multilayer with capacitor.ti. and(anode)) and(cathode	USPAT; US-PGPUB; JPO	2004/10/19 09:36
–	0	capacitor near package and(fan with plate)	USPAT; US-PGPUB; JPO	2004/10/19 09:36
–	15565	fan with plate	USPAT; US-PGPUB; JPO	2004/10/19 09:36
–	741203	electrode wit fan with plate	USPAT; US-PGPUB; JPO	2004/10/19 09:36
–	1680086	h	USPAT; US-PGPUB; JPO	2004/10/19 09:36
–	105	electrode with fan with plate	USPAT; US-PGPUB; JPO	2004/10/19 09:42
–	37	capacitor.ti. and(plate near assembly)	USPAT; US-PGPUB; JPO	2004/10/19 09:43
–	1	multi adj layer with capacitor.ti. and(second near plate)	USPAT; US-PGPUB; JPO	2004/10/19 09:45
–	0	multi adj layer with capacitor.ti. and(rectangular near volume)	USPAT; US-PGPUB; JPO	2004/10/19 09:45
–	24	multi adj layer with capacitor.ti. and(rectangular)	USPAT; US-PGPUB; JPO	2004/10/19 09:53

-	0	multi adj layer with capacitor.ti. and(anode)	USPAT; US-PGPUB; JPO	2004/10/19 09:53
-	2	multi adj layer with capacitor.ti. and(positive near electrode)	USPAT; US-PGPUB; JPO	2004/10/20 07:29
-	49	capacitor.ti. and(terminal$1 with first near polarity)	USPAT; US-PGPUB; JPO	2004/10/20 07:29
-	34	capacitor.ti. and(terminal$1 with first near polarity)) and(terminal$1 with second near polarity	USPAT; US-PGPUB; JPO	2004/10/20 08:38
-	16	((capacitor.ti. and(terminal$1 with first near polarity)) and(terminal$1 with second near polarity)) and(positive and negative)	USPAT; US-PGPUB; JPO	2004/10/20 08:12
-	0	(((capacitor.ti. and(terminal$1 with first near polarity)) and(terminal$1 with second near polarity)) and(motherboard)) and(voltage near regulat$3)	USPAT; US-PGPUB; JPO	2004/10/20 08:38
-	1	((capacitor.ti. and(terminal$1 with first near polarity)) and(terminal$1 with second near polarity)) and(motherboard)	USPAT; US-PGPUB; JPO	2004/10/20 08:40
-	1	(((capacitor.ti. and(terminal$1 with first near polarity)) and(terminal$1 with second near polarity)) and(motherboard)) and(chip)	USPAT; US-PGPUB; JPO	2004/10/20 08:40
-	0	(((((capacitor.ti. and(terminal$1 with first near polarity)) and(terminal$1 with second near polarity)) and(motherboard)) and(chip)) and(memory)) and(voltage)	USPAT; US-PGPUB; JPO	2004/10/20 08:41
-	1	(((((capacitor.ti. and(terminal$1 with first near polarity)) and(terminal$1 with second near polarity)) and(motherboard)) and(chip)) and(memory)) and(power)	USPAT; US-PGPUB; JPO	2004/10/20 08:45
-	74338	system.ti. and(regulat$3)	USPAT; US-PGPUB; JPO	2004/10/20 08:45
-	560	system.ti. and(regulat$3)) and(motherboard	USPAT; US-PGPUB; JPO	2004/10/20 08:45
-	309	((system.ti. and(regulat$3)) and(motherboard)) and(chip)	USPAT; US-PGPUB; JPO	2004/10/20 08:45
-	281	(((system.ti. and(regulat$3)) and(motherboard)) and(chip)) and(memory)	USPAT; US-PGPUB; JPO	2004/10/20 08:45
-	257	((((system.ti. and(regulat$3)) and(motherboard)) and(chip)) and(memory)) and(bus)	USPAT; US-PGPUB; JPO	2004/10/20 08:46
-	15	(((((system.ti. and(regulat$3)) and(motherboard)) and(chip)) and(memory)) and(bus)) and(synchronous near dynamic)	USPAT; US-PGPUB; JPO	2004/10/20 08:49
-	8	((((((system.ti. and(regulat$3)) and(motherboard)) and(chip)) and(memory)) and(bus)) and(synchronous near dynamic)) and(capacitor)	USPAT; US-PGPUB; JPO	2004/10/20 08:47
-	0	(((((capacitor.ti. and(terminal$1 with first near polarity)) and(terminal$1 with second near polarity)) and(motherboard)) and(chip)) and(memory)) and(bus)	USPAT; US-PGPUB; JPO	2004/10/20 08:49
-	75	system.ti. and(regulat$3)) and(memory with synchronous near dynamic	USPAT; US-PGPUB; JPO	2004/10/20 08:50
-	0	((system.ti. and(regulat$3)) and(memory with synchronous near dynamic)) and(dynamic near randon near access near memory)	USPAT; US-PGPUB; JPO	2004/10/20 08:51
-	66	((system.ti. and(regulat$3)) and(memory with synchronous near dynamic)) and(dynamic near random near access near memory)	USPAT; US-PGPUB; JPO	2004/10/20 08:51